In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 3, lines 3 to 13 as follows:

--Traditionally, critical I/O timing specifications make it necessary for designers to comprehend all of the following design ~~characteristics"(a)~~ characteristics: (a) I/0 interface design/architecture; (b) simplified clock distribution; (c) master/slave protocols; (d) self-clocking techniques including the use of analog or digital phase locked loop functions to create alignments between I/O circuit ~~&~~ and process; (e) I/O buffers designed for low voltage-temperature performance variation; (f) rigid process controls; (g) I/O test screening; and (h) speed sort parts by I/O speeds/application. All these design and application considerations involve sophisticated design/process practices and/or compromises in design/process.--

Rewrite the paragraph at page 5, lines 11 to 19 as follows:

--In the program mode, incoming PData In 107 is latched into the PData flip-flop 102 and programmed into the eFuse element on the occurrence of one or more program pulses initiated at Program input 110. PData Out passes to the next eFuse cell via path 116. In the program mode PData Out is passed through multiplexers 104 and 105 and is latched into the CData flip-flop ~~102~~ 103. The voltage VPP 109 is the programming power source. Program data is passed serially to the next cell in the chain at PData Out line 116.--

Rewrite the paragraph at page 10, lines 5 to 24 as follows:

--Figure 3 illustrates a high-speed I/O buffer block 300 for a processor device with boundary 303 showing the associated input and output register stages and pertinent signal and specification definitions. System clock 310 ~~is~~ passes to input and output portions of the circuit by clock distribution spine 304. Most significant among high-speed buffer I/O blocks are the external memory interface (EMIF) function, but the clock tuning adjustments described here are by no means limited to EMIF. The I/O buffer stage 300 has an input portion buffering data input 301 and output portion buffering data output 302. Data input 301 passes to register 311 and is clocked by input clock 313. Input clock 313 is a delayed form of system clock 310. Registered data input is denoted by the label incoming data 307. Delay element 315 is controlled by eFuse program inputs 317. Outgoing data 308 is passed to register 312, which is clocked by output clock 314. Output clock 314 is a delayed form of system clock 310. Delay element 316 is controlled by eFuse program inputs 318. Data from register 312 is buffered and passed to data output node 302.--